

In the specification:

Paragraph 18:

Referring now to FIG. 3, a cross-sectional view of a shallow-trench isolated MOS transistor 50 illustrates the features of the present invention. Shallow-trench isolated MOS transistor 50 is formed in silicon substrate 52 between two shallow portions shown in FIG. 3 of an annular trench isolation structures filled with deposited silicon dioxide 54 as in the prior-art shallow-trench isolated MOS transistor of FIG. 2. Gate oxide layer 56 insulates polysilicon gate 58 from the surface of substrate 52.

Paragraph 19:

Unlike the prior-art shallow-trench isolated MOS transistor of FIG. 2, a sidewall implant 60 is formed in the walls of the isolation trenches prior to the deposition of the oxide fill regions 54. The implant is performed at an angle so that it penetrates the sidewalls of the trenches. The substrate may be rotated or other techniques may be employed to assure implanting all four of the sidewalls shown in FIG. 3 as well as the sidewalls of the front and rear portions of the trench lying outside of the plane of FIG. 3.

Paragraph 22:

Referring now to FIG. 4A, substrate 52 is shown after formation of annular isolation trenches 62. As will be appreciated by persons of ordinary skill in the art, isolation trenches 62 are is formed using conventional masking and etching techniques to a depth of about 400nm, after which the mask layer is removed using conventional semiconductor processing techniques.

Paragraph 23:

As shown in FIG. 1, sidewall implants 60 are formed in the side and bottom walls of isolation trenches 62. As will be appreciated by persons of ordinary skill in the art, sidewall implants 60 may be formed using an angled ion-implant process during which the substrate 52 may be rotated as known in the art to assure coverage of all of the sidewalls of the isolation trenches 62. FIG. 4A shows the structure existing after the performance of the sidewall implant step for one type of transistor before removal of implant mask layer 64.

Paragraph 25:

Referring now to FIG. 4B, implant mask layer 64 has been removed. Silicon dioxide regions 54 have been formed in trenches 62 using conventional CVD or PECVD techniques and the surfaces of silicon dioxide regions 54 and the top surface of substrate 52 have been planarized using conventional CMP techniques. Note that, as an artifact of the planarizing process and oxide etching steps, the edges of the top surface of silicon dioxide regions 54 lie below the edges of isolation trenches 62.

Paragraph 26:

Referring now to FIG. 4C, gate oxide layer 56 and polysilicon gate layer 58 have been formed and defined using conventional photolithographic and semiconductor processing techniques. Source and drain regions (outside of the plane of the cross-section of FIG. 4C and therefore shown as dashed lines 66) are implanted using the edges of the gate 58 as a mask in a conventional self-aligned gate process sequence. Note that the polysilicon gate regions adjacent to the edges